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FREEDOM TO OPERATE SEARCH

Title: Digital signal processing for PLC communications having communication frequencies

Data Submitted to:

Address:

Email:

Client Reference No:

Patent Number: US8737555

Priority Date: 22 Dec 2011

Assignee: Landis+Gyr Technologies, Llc Date:

Claims:

1. 1. A circuit-based apparatus comprising:

a transceiver circuit configured and arranged to communicate over power distribution lines that carry power using alternating current (AC);

one or more processing circuits configured and arranged to provide an analog to digital converter module configured to generate an input digital signal from an analog signal that was received at the transceiver circuit;

a decimator module configured to produce, in response to a variable decimation rate, a decimated input digital signal;

a reference signal generator module configured to generate a reference signal having a frequency responsive to the decimation rate; and

a decimation modification module configured and arranged to modify, in response to an indication of change in a phase difference between the reference signal and the AC, the decimation rate to counteract the phase difference.

Feature to Search

E1. A circuit-based apparatus comprises a transceiver circuit configured and arranged to communicate over power distribution lines that carry power using alternating current (AC).

E2. A circuit-based apparatus comprises one or more processing circuits configured and arranged to provide an analog to digital converter module configured to generate an input digital signal from an analog signal that was received at the transceiver circuit.

E3. A circuit-based apparatus comprises a decimator module configured to produce, in response to a variable decimation rate, a decimated input digital signal; A reference signal generator module configured to generate a reference signal having a frequency responsive to the decimation rate.

E4. A decimation modification module configured and arranged to modify, in response to an indication of change in a phase difference between the reference signal and the AC, the decimation rate to counteract the phase difference.

Search Strategy

Database: AcclaimIP, USPTO, Patentscope, Espacenet, Google Patents, Inpass.

Keywords:

Set 1	Analog signal, digital signal, analog current, digital current
Set 2	Power distributed lines, power lines, power line communication
Set 3	Phase difference, phase error
Set 4	Variable decimation, adjustable decimation

US CLASSIFICATIONS

375/260 Plural channels for transmission of a single pulse train

369/59.21 Including sampling or A/D converting

375/324 Particular demodulator

INTERNATIONAL CLASSIFICATIONS

H04L27/28 with simultaneous transmission of different frequencies each representing one code element

G11B7/00 Recording or reproducing by optical means, e.g. recording using a thermal beam of optical radiation, reproducing using an optical beam at lower power; Record carriers therefor

H04L27/22 Demodulator circuits; Receiver circuits

Search Results

Reference 1:

Patent/Publication Number US8223859

Title: Method and apparatus for a multi-tone modem

Assignee/Applicant: Ikanos Communications, Inc.

Filing Date: 25 Jun 2008

Priority Date: 25 Jun 2008

Also Published as: US20100002755, WO2010008492

Relevant Excerpt E1	**IN CLAIMS:** 1. A multi-tone modem with a plurality of shared and discrete components forming a transmit path and a receive path configured to couple to **an alternating current (AC) power line wired communication medium to communicate at least one multi-tone modulated communication channel thereon.**
Relevant Excerpt E2	**IN CLAIMS:** 6. The multi-tone modem of claim 1, wherein the at least at least one configurable **frequency up converter** component comprises: **at least one of a digital up converter and an analog up converter.**
Relevant Excerpt E3	**IN CLAIMS:**
	23. The means of claim 16, wherein the multi-tone modulating and demodulating means and the selectable up and down converting means further comprise: means for multi-tone modulating and demodulating two discrete communication channels at the base band frequency range; and means for up and down converting the two discrete communication channels between the base band frequency range and a corresponding one of two discrete selected communication bands, thereby supporting communications on any selected two of a plurality of discrete frequency bands supported by the wired communication medium.
Relevant Excerpt E4	Not Disclosed

Reference 2:

Patent/Publication Number US8456977 **Title:** Digital PLL circuit, information readout device, disc readout device, and signal processing method **Assignee/Applicant:** Renesas Electronics Corporation **Filing Date:** 12 Oct 2010 **Priority Date:** 12 Oct 2010 **Also Published as:** US20120087225	
Relevant Excerpt E1	Not Disclosed
Relevant Excerpt E2	**IN CLAIMS:** 1. A digital PLL (phase locked loop) circuit, comprising:
	an AAF (anti aliasing filter) that limits a frequency bandwidth of an input RF (radio frequency) signal on a basis of a given cutoff frequency; **an ADC (analog to digital converter) that samples an output signal of the AAF on a basis of a given sampling frequency;**
Relevant Excerpt E3	**IN CLAIMS:** 3. The digital PLL circuit according to claim 1, wherein the down converter includes a low-pass filter that can change a cutoff frequency, and **a decimator that decimates an output signal of the low-pass filter.**
Relevant Excerpt E4	Not Disclosed

Reference 3:

Patent/Publication Number US7792220 **Title:** Demodulator system and method **Assignee/Applicant:** Sigmatel, Inc. **Filing Date:** 19 Dec 2006 **Priority Date:** 19 Dec 2006 **Also Published as:** US20080144743	
Relevant Excerpt E1	Not Disclosed
Relevant Excerpt E2	**IN CLAIMS:** 1. A demodulator system comprising: **an analog-to-digital converter (ADC) configured to sample a**
	modulated signal and to output a digital signal; a Coordinate Rotation Digital Computer (CORDIC) mixer coupled to an output of the ADC, the CORDIC mixer to generate an Inphase (I) signal and a Quadrature (Q) signal based on the digital signal output by the ADC and further based on an input frequency;

Relevant Excerpt E3	**IN CLAIMS:** 8. A demodulator system comprising: a Coordinate Rotation Digital Computer (CORDIC) mixer to generate an Inphase (I) signal and a Quadrature (Q) signal based on a modulated input signal and an input frequency; **a decimator to perform decimation of the I signal and the Q signal at an adjustable decimation rate;** a phase detector to receive a pilot signal and including decimation rate logic to generate a control signal to adjust the decimation rate based on the pilot signal; and a demodulation stage to demodulate a filtered output of the decimator, wherein the demodulation stage includes a CORDIC demodulator.
Relevant Excerpt E4	**IN CLAIMS:** 21. The demodulator system of claim 20, **wherein the symbol recognition logic includes logic to modify a value of the phase accumulator based on a difference between an adjusted sample and the nearest predetermined phase value.**

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